PHASE LOCKED LOOP CIRCUIT FOR A FRACTIONAL-N FREQUENCY SYNTHESIZER

Abstract of the Disclosure

A phase locked loop (PLL) circuit for synchronizing a fractional-N frequency synthesizer employs an interpolation method. However, by limiting the number of delay signals to 8 and by using the phase accumulation method during the four cycles of the feedback signal in response to the fractional division ratio data, it is possible to perform the divide-by-fraction, for example, F/32 (F=0, 1, 2, ..., 31). According to the present invention, the substrate noise is decreased in comparison with the phase interpolation method using 32 delay signals, and the PLL circuit is insensitive to physical error. While a method of accumulating the phases during 32 cycles is in need of an additional compensating circuit so as to minimized fractional spurious, the PLL circuit of the present invention does not require additional compensation circuits, by employing the inventive method of accumulating phases during a predetermined number of cycles, for example four.

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